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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,563	08/16/2007	Lily Zhao	US04 0110 US2	8298
65913	7590	08/20/2009	EXAMINER	
NXP, B.V. NXP INTELLECTUAL PROPERTY & LICENSING M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			PATEL, ISHWARBHAI B	
			ART UNIT	PAPER NUMBER
			2841	
			NOTIFICATION DATE	DELIVERY MODE
			08/20/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/588,563	ZHAO ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 May 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) 16-24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 August 2007 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>8/3/06</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of group I, specie I, claims 1-15 in the reply filed on May 29, 2009 is acknowledged. The traversal is on the ground(s) that the condition that invention or groups of inventions which are not so linked as to form a single general inventive concept under PCT rule 1311 is incorrectly applied and there would be no undue burden in examining these alleged group.

This is not found persuasive because: as explained in the previous action both of the group contain claims having different special technical features and search for both the invention will be burdensome to the Examiner. Further, as applied to the claim rejection, the claimed structure, as disclosed by Arndt (US Patent No. 6,232,564), is known in the art.

The requirement is still deemed proper and is therefore made FINAL.

Specification

2. The disclosure is objected to because of the following informalities: The specification is not arranged as per the guideline. Applicant is requested to follow the guide lines suggested as follow:

Appropriate correction is required.

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
- (e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
- (f) BACKGROUND OF THE INVENTION.
 - (1) Field of the Invention.
 - (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (g) BRIEF SUMMARY OF THE INVENTION.
- (h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
- (i) DETAILED DESCRIPTION OF THE INVENTION.
- (j) CLAIM OR CLAIMS (commencing on a separate sheet).
- (k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
- (l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

3. The abstract of the disclosure is objected to because:

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words and to be provided on a separate page.

Correction is required. See MPEP § 608.01(b).

4. The disclosure is objected to because of the following informalities:

(a) Reference numeral are not correct for the first, second and third layer, page 3, line 29-33 and page 4, line 1-6.

Appropriate correction is required.

(b) Figures are identified as 2A, 2B..... etc. in the figures, whereas, they are identified as 2a, 3a, in specification. Appropriate changes to be made in the figures or specification.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arndt (US Patent No. 6,232,564).

Regarding claim 1, Arndt in figure 3 discloses a multilayer circuit board comprising: a first layer (24); a fourth layer substantially parallel to the first layer (though not explicitly shown, it would have been obvious to have a board with more layers, including a fourth layer, column 3, line 30-40, in order to have desired wiring density); a plurality of electrical contacts (contacts ones with blank circle and the other with smaller circle within circle) formed within the first layer of the multilayer circuit board and disposed in a first grid having, a first subset (contact with smaller circle within circle, see

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figure) of the plurality of electrical contacts for routing within the first layer and a second subset (ones with blank circle) of the plurality of electrical contacts for routing within the fourth layer and, a plurality of vias (via for example 42) formed between the first layer and fourth layer and each disposed adjacent at least one of the second subset of the plurality of electrical contacts (see figure), the plurality of vias having a spacing between each pair thereof larger than a smallest spacing between adjacent electrical contacts of the plurality of electrical contacts (see figure).

Regarding claim 2, the modified board of Arndt discloses all the features of the claimed invention including the plurality of vias having spacing larger than the that of the first grid but does not explicitly disclose the vias have a spacing of at least 1.1 times the first grid spacing.

However, the spacing will be decided based on the space available on the board to have better routing of the trace and optimize the surface area.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified board of Arndt with vias having a spacing of at least 1.1 times the first grid spacing, in order to optimize the surface area of the board.

Regarding claim 3, the modified board of Arndt further discloses electrical contacts of the plurality of electrical contacts within the first grid alternate between the

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first subset of electrical contacts and the second subset of electrical contacts (see figure).

Regarding claim 4, the modified board of Arndt further discloses the first grid comprises a Cartesian grid comprising columns and rows (see figure), where each row and each column comprises alternating electrical contacts from the first subset and the second subset (see figure) the plurality of vias disposed in a second grid comprising columns and rows having a substantially second pitch between adjacent vias (see figure), where electrical contacts for the first subset are routed within the first layer using one of a plurality of first electrical traces and electrical contacts for the second subset are routed along the fourth layer using one of a plurality of second electrical traces (see figure, one connected with traces and the other with vias).

Regarding claims 5 and 6, the modified board of Arndt discloses all the features of the claimed invention including the plurality of vias having spacing larger than the that of the first grid as applied to claim 1 above but does not explicitly disclose pitch of the vias disposed in a second grid is at least 1.1 times larger than the pitch of the electrical contacts disposed in the first grid (claim 5) or pitch of the vias disposed in a second grid is approximately the square root of two times larger than the pitch of the plurality of electrical contacts disposed in the first grid (claim 6).

However, the spacing will be decided based on the space available on the board to have better routing of the trace and optimize the surface area.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified board of Arndt with pitch of the vias disposed in a second grid is at least 1.1 times larger than the pitch of the electrical contacts disposed in the first grid (claim 5) and pitch of the vias disposed in a second grid is approximately the square root of two times larger than the pitch of the plurality of electrical contacts disposed in the first grid (claim 6), in order to optimize the surface area of the board.

Regarding claim 7, the modified board of Arndt discloses all the features of the claimed invention including first grid and the second grid are provided at angle but does not disclose the angle between the first grid and the second grid is approximately 45 degrees.

However, the angle between the grid will be selected to have better routing of the traces on the surface of the board to optimize the available area of board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified board of Arndt with the angle between the first grid and the second grid is approximately 45 degrees, in order to optimize the surface area of the board.

Regarding claim 8, the modified board of Arndt further discloses the first subset of the plurality of electrical contacts comprise bond pads (see figure).

Regarding claim 9, it would have been obvious to provide the vias disposed at opposite sides of adjacent electrical contacts belonging to the second subset, in order to optimize the surface area of the board.

Regarding claim 10, the modified board of Arndt further discloses a first substrate, where the first layer is disposed within a first outside surface of the first substrate and where the plurality of vias are drilled through the first substrate to a second other outside surface thereof, where the fourth layer is disposed within the second other outside surface of the first substrate (as applied to claim 1 above).

Regarding claim 11, the modified board of Arndt further discloses a core layer disposed between the first and fourth layers (as it is a multilayer board), wherein the core layer comprises a plurality of other layers that are substantially parallel to the first layer and the fourth layer and the plurality of other layers comprising a plurality of non-conducting areas that surround the plurality of vias (obvious to have non conductive area around vias to isolate them).

Regarding claim 12, the modified board of Arndt discloses all the features of the claimed invention as applied to claim 11 above including via and non-conducting area around the via but does not disclose an electrically conducting material disposed about the plurality of non-conducting areas for reducing a bi-planar cross-talk between the first layer and the fourth layer.

However, providing electrically conducting material in the form of shielding material is old and known in the art to reduce noise.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified board of Arndt with an electrically conducting material disposed about the plurality of non-conducting areas for reducing a bi-planar cross-talk between the first layer and the fourth layer, in order to reduce noise, as is old and known in the art.

Regarding claims 13 and 14, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified board of Arndt discloses with the plurality of non-conducting areas are disposed in such a manner that vias formed on adjacent electrical contacts from the plurality of electrical contacts are other than supported due to overlap between adjacent non-conducting areas (claim 13) and each of the plurality of non-conducting areas is free of all other electrical contact other than a via disposed therein once the multilayer circuit board is formed (claim 14), in order to have better performance of the board.

Regarding claim 15, the modified board of Arndt further discloses each via is adjacent at least two electrical contacts (see figure).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shenoy (US Patent No. 6,198,635) in figure 4 discloses contact array on a layer of the board.

Miller (US Patent No. 6,762,366) discloses contact array design on different layers of a printed circuit board.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on (571) 272 1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ibp
August 15, 2009

/Ishwar (I. B.) Patel/
Primary Examiner, Art Unit 2841